A MOSFET alternative for switching frequencies up to more than 300 kHz

High-speed 600V IGBT in NPT technology

Because of its many advantages over PT technology, NPT technology has gained increasing acceptance for IGBTs with breakdown voltages of over 1 kV. Siemens is now continuing this logical progression with a new 600V NPT product range, providing the user with such characteristics as minimal dynamic losses and unbeatable ruggedness at only narrow dynamic parameter tolerances even in this voltage category. Because of their low dynamic losses, the new NPT-IGBT are penetrating fields of application that were hitherto the domain of the MOSFET. They therefore represent – depending on switching topology – a cost-effective alternative to MOSFET up to switching frequencies of 300 kHz and beyond. This article introduces the new 600V NPT-IGBT with their main electrical characteristics and gives some idea of the capabilities of these devices as exemplified by some typical applications.

by M. März, A. Knapp, M. Billmann

Fig. 1 shows the essential difference between an NPT (non-punch-through) and a PT (punch-through) IGBT. The layout of the individual transistor cells on the front side of the chip is the same in each case. In the PT-IGBT, a highly doped n^+-type buffer layer and a low doped n-type layer are epitaxially grown on a p-doped substrate. The space-charge region in the blocked state extends into the n^+ buffer layer.

By contrast, in the NPT concept the reverse voltage is applied to a single homogeneous, low-doped n-layer without buffer. The p-layer on the collector side is only introduced by means of an implantation step after backside grinding of the wafer.

The n^--layer must not be significantly thicker than is necessary to provide the blocking capability, as any additional thickness would increase the on-state saturation voltage (= $V_{ce,sat}$).

For IGBT with 600V reverse voltage, the required wafer thickness is approximately 100 µm, which represents an enormous technical challenge in manufacturing terms. For this reason the NPT concept and its advantages had hitherto been restricted to the 1000V-plus categories.

100 µm wafer – a milestone on the way to the 600V NPT-IGBT

Siemens took up the challenge and is now successful in fabricating 100µm wafers in productive scale and with high yields. The basic steps in achieving this included measures to reduce the warpage of the thin Si-wafer from an original value of around 15 mm to a production-tolerable figure of less than 5 mm. Improvements in the wafer grinding equipment were just as important here as adaptations of the passivation layer of the front side and reducing deformations caused by backside metallization [1]. The implementation of a large number of individual measures enabled warpages to be reduced to less than 1 mm.

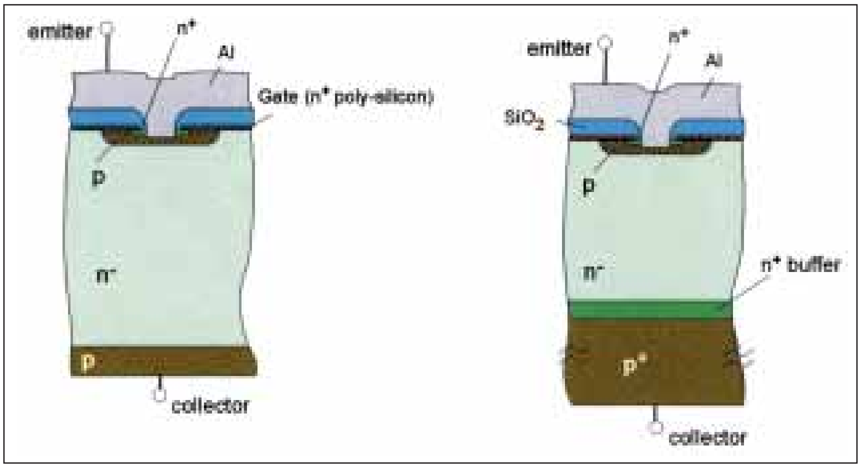

Fig. 1: Cross-section of NPT-IGBT (left) and PT-IGBT (right)

Excellent ruggedness through NPT technology

The implantation step for producing the p-emitter can be very precisely monitored during production. Consequently, a much more accurate adjustment and significantly better reproducibility of the p-emitter can be achieved than is possible with the PT concept where there are considerable technological problems in monitoring the doping concentrations of the p^+-substrate and n^+-buffer, resulting in variances in the charge carrier concentration in the drift region and consequently considerable variances in the tail currents. Other manufacturing variances are introduced by the adjustment of the charge carrier lifetime (life-time-killing) required by the PT concept. This means that with the NPT concept the user enjoys much lower static and dynamic parameter variations. In addition, only a very low emitter efficiency is required to achieve a saturation voltage of somewhat less than 2V. This is combined with a low tail current, a high switching speed and consequently minimized dynamic losses. The low switching losses are achieved without additional lifetime reducing measures, such as irradiation with electrons, high-speed neutrons or X-rays, or diffusion of heavy metals such as platinum, as is normal with the PT concept. All in all, the NPT-IGBT can therefore be manufactured with fewer and more readily controllable process steps.

Fig. 2 impressively demonstrates the improvement in the dynamic characteristics by comparing a new NPT S-IGBT with a commercially available Siemens PT-IGBT of identical area and cell design.

As the switching characteristics show, with NPT technology the turn-off losses are reduced by more than a factor of 3..5 compared to the PT variant. This is because of a significantly faster current fall time of less than 50 ns and a virtually non-existent current tail. The latter being both of very short duration (less than 500 ns) and is only starting at below 10% of the operating current.

A deciding advantage of the NPT S-IGBT is that the very low current tail remains absolutely stable over the whole temperature range. With PT-IGBT in contrast, the tail losses steeply increase with the chip temperature – a fact which is very critical in practice, especially at high switching frequencies.

In addition to reducing the switching losses, another development objective for the new 600V IGBTs was to reduce the threshold voltage from 5.5V to a typical value of 4V. This has implications for the typical drive conditions in switch mode power supplies with gate voltages of generally no more than 10...12V. The output characteristic in Fig. 3 indicates that the S-IGBT can still be reliably turned on even at these gate voltages. Another favorable aspect of the S-IGBT is the slightly positive temperature coefficient of 3 mV per °C, a basic prerequisite for problem-free paralleling. The threshold voltage of typically 4V has been ensured by technological measures which do not impact the maximum ratings (e.g. maximum permissible gate voltage) and more particularly involve no penalties in terms of IGBT ruggedness. The new high-speed 600V NPT-IGBT product range therefore exhibits the customary and appreciated NPT-IGBT characteristics such as absence of latch-up and a high degree of short circuit protection.

For the latch-up test (Fig. 4, left) the device is turned off at maximum permissible gate voltage – by the high current (approximately 10 times the rated current) resulting from the output characteristic – with high di/dt in response to negative gate voltage values. It can be seen that the IGBT overcomes these extreme conditions without the parasitic thyristor structure being activated.

For the short circuit test, the IGBT is turned on to an existing short circuit and not turned off again until after 20 µs (guaranteed value 10µs). This extremely long time span gives even the simplest protection circuitry sufficient time to detect the short circuit and turn off the IGBT. During the short circuit time the IGBT must simultaneously withstand the full voltage (400V) and a current some 7 times higher than the rated current (at V_{ge} = 15V)! Under the test conditions shown in Fig. 4, this means a peak power dissipation in the chip of around 100 kW!

However, the 100 µm IGBT withstands even this extreme loading in the usual exemplary manner of Siemens NPT-IGBT.

Fig. 5 shows the current product range of the new Siemens 600V S-IGBTs which will supersede the 600V PT types in the medium term. The lower end of the rated current range has been extended to include two chips rated 2A and 4A respectively, and new packages are also included in the form of the D-Pak and I-Pak. In addition to devices in leaded TO-220 (SGP..) and I-Pak (SGU..) packages, the relevant SMD variants TO-220SMD (SGB..) and D-PAK (SGD..) are naturally also available; Duo-Pak devices (= IGBTs with inverse-parallel freewheeling diode) will follow.

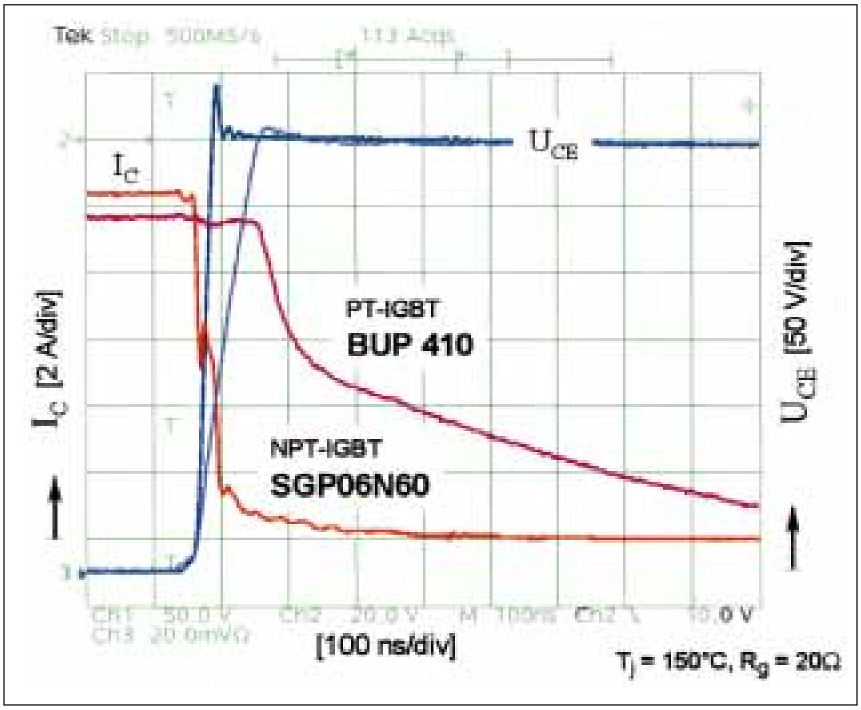

Fig. 2: Turn-off behavior of an NPT S-IGBT compared to a PT-IGBT of identical chip area (BUP410)

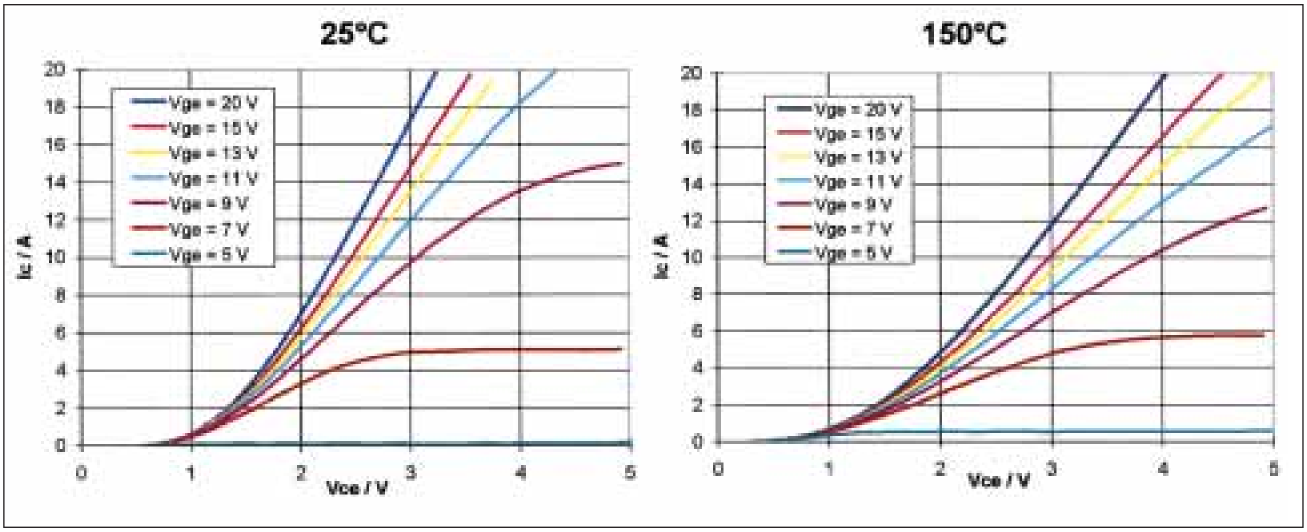

Fig. 3: Output characteristic $I_C(V_{CE})$ of S-IGBT SGP06N60 at T_j = 25°C and 150°C

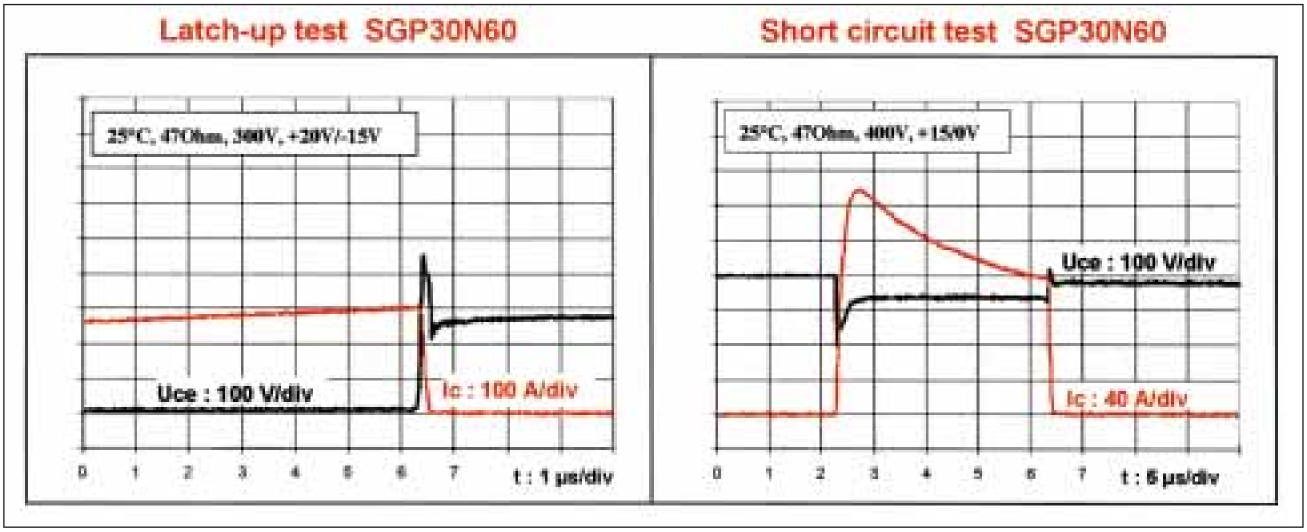

Fig. 4: Latch-up (left) and short circuit behavior (right) of a 600V NPT S-IGBT

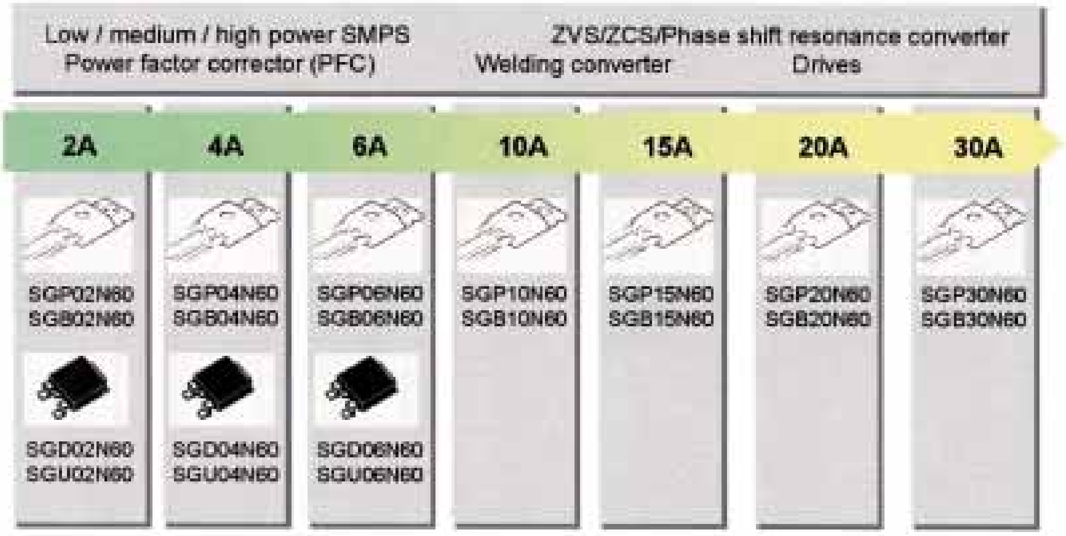

Fig. 5: 600V S-IGBT product range (current ratings at 100°C case temperature)

II. S-IGBTs conquer new fields of application

In virtually all fields of application for high-speed, high-voltage switches, MOSFET and IGBT devices have now completely ousted bipolar transistors. Whereas for a long time the area of low switching frequencies (<50 kHz) has appeared to be the domain of the IGBT, modern high-speed IGBTs are now beginning to compete with MOSFETs even in their traditional fields of application - switch mode power supplies. High-speed IGBTs are making inroads wherever their specific advantages can be fully utilized, these being:

a. excellent ruggedness (short circuit protection, latch-up free, avalanche rated), and

b. superior on-state characteristics at high currents.

Fig. 6 shows current-carrying capability versus switching frequency for the new Siemens S-IGBT and CoolMOS™ families in comparison with conventional Power-MOSFET. The current-carrying capability describes the r.m.s. switch current that can be handled per mm^2 chip area at a particular switching frequency of the device, without exceeding the assumed power dissipation density. Fig. 6 applies to the switching conditions usually found in conventional single-ended converters, i.e. for "hard" switching without off-commutation of a diode at turn-on, and under the constraint of a power dissipation density (=power dissipation/chip area) of 5W/mm^2. Essentially, the higher the current density and hence the power dissipation-density (not the absolute power dissipation!) the more the excellent on-state characteristics of the IGBT come into play.

Because of their superior current-carrying capability and ruggedness, the IGBTs have gained greatest acceptance in their traditional application field of drive systems.

However, the development of the ultra-fast S-IGBT has now drastically extended this field. As Fig. 6 shows, the S-IGBT is superior in terms of current-carrying capability to the standard MOSFET – depending on power dissipation density – up to 300 kHz and beyond, and to the Cool MOS™ under typical operating conditions up to around 100 kHz.

These high possible operating frequencies make the S-IGBTs ideally suitable for switch mode power supplies and power factor corrector (PFC) applications. For active power factor correction, a step-up converter topology in continuous flow operation is generally used (see Fig. 7), in which the conceivably usable switching frequency – determined by the characteristics of the currently available high-speed diodes – is limited to about 40...100 kHz. Otherwise the losses caused by the turn-off current peaks of the diode (D1) in the transistor (T1) become unacceptably high. In the switching frequency range quoted, an S-IGBT can replace a standard MOSFET with 3-4 times larger chip area for the same power dissipation and therefore represents an cost-effective alternative to the standard MOSFET. In addition, because of the smaller chip area, the input capacitances are also significantly smaller than those of the standard MOSFET which is to be replaced, which means that the S-IGBT requires a much lower driver power.

The window selected for the gate-emitter threshold voltage of 3V...5V @ 25°C represents an ideal compromise between high noise immunity even without negative OFF-state gate voltage, compatibility with standard MOSFET drive ICs and high output even at 12V gate voltage. Consequently, in many cases an existing MOSFET can be directly replaced by an S-IGBT. The only qualification is that in the event of the risk of negative undershoots of the collector-emitter voltage (e.g. because of parasitic oscillations), a low-current 600V diode must be connected back-to-back with the IGBT, as the latter does not have the inverse-parallel diode inherent in the MOSFET structure.

Taking the example of a flyback converter (cf. T2 in Fig. 7) with a switching frequency of 100 kHz, Fig. 8 shows a power dissipation comparison between a standard MOSFET and an S-IGBT of identical chip area. It is apparent that the higher switching losses of the IGBT are more than compensated by the drastically reduced on-state losses, so that – in spite of a switching frequency of 100 kHz – the overall IGBT losses are barely more than half the

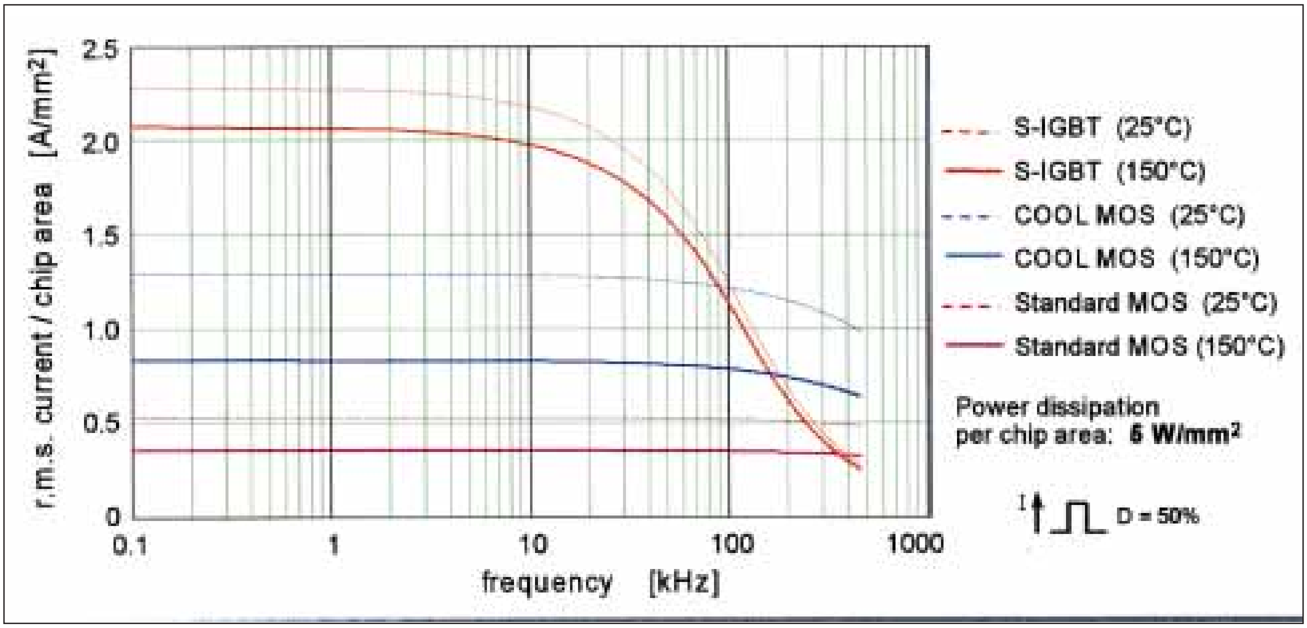

Fig. 6: Current-carrying capability per chip area as a function of the switching frequency; standard MOSFET, COOL MOS™ power FET and S-IGBT compared

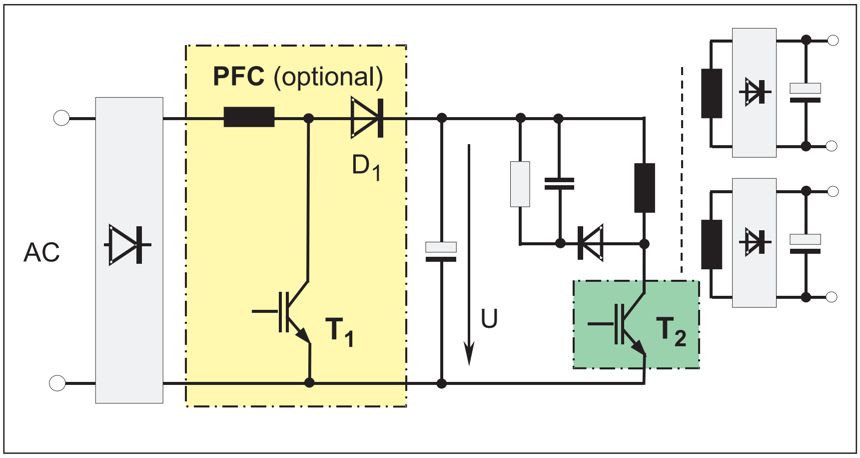

Fig. 7: Forward or flyback converters are the most common topologies for switch mode power supplies up to 250W. A large proportion of power supplies will in future have to be equipped with a power factor corrector (PFC)

MOSFET losses. As shown in Fig. 6, the current-carrying capability of an S-IGBT at 100 kHz is approximately twice that of a standard MOSFET, the IGBT of identical chip area used in Fig. 8 for comparison therefore being by no means the optimum solution. Rather the chip area could be reduced by a factor of 2-3 (!) – without significantly affecting the overall power dissipation – which makes the S-IGBT extremely interesting in this application, not only in terms of power dissipation but also in terms of cost-effectiveness.

Because of their better utilization of the switches and inductive components, bridge circuits predominate in the power range above 250 W. In addition to drive systems, there is here a wide field of applications in the area of high-power switch mode power supplies, uninterruptible power supplies (UPS), high-voltage converters for microwave and medical systems, welding equipment (typ. 1..20 kW) and induction heating systems (2 kW.. 1.5 MW). In order to avoid the no longer controllable losses in the event of hard commutation of the bridge diodes, or even merely to minimize the switching losses, soft or resonant switching principles are used virtually exclusively at higher switching frequencies. One of the currently most advanced methods is the phase-shift ZVS technology, whereby the power is controlled via a phase shift in the bridge drive signals and zero-voltage switching (ZVS) of the switches is achieved. Because of its major advantages such as low switching losses, low reactive power, very few additional passive components and relatively simple drive arrangement, this method is currently gaining rapid acceptance in many fields of application.

The performance of the new S-IGBT under ZVS conditions is demonstrated using the example of the simplified half-bridge test circuit shown in Fig. 9.

For switching frequencies in the inductive range of the bridge shunt arm, the IGBT in this circuit is essentially turned on at zero voltage (ZVS). At turn-off, however, the switches have to handle a current that is approximately 3 to 4 times the r.m.s. switch current.

A 6A S-IGBT with a chip area of only about 5 mm² is capable, under these operating conditions, of handling current peaks of over 15 A at a switching frequency of more than 200 kHz (!). This corresponds to a transmittable power of well over a kilowatt at approximately 35 W power dissipation per switch. Fig. 10 shows the turn-off behavior of the S-IGBT under the specified conditions. The circuit was operated without snupper capacitors in parallel with the IGBTs.

Also under ZVS operating conditions, the S-IGBT exhibit an extremely low tail current. The tail is nearly temperature independent so that the NPT S-IGBT operate with absolute stability even at a chip temperature of 150°C.

On the other hand, ultra-fast PT-IGBTs from competitors – despite a significantly reduced peak current (see Fig. 10) - exhibited a thermal "runaway" that is highly critical in practice. This is caused by the very marked increase in tail losses with chip temperature which is typical of PT-IGBTs. With two 6A S-IGBT, powers of more than 300 W are still transmittable with an output stage efficiency of over 80% even at a switching frequency of 500 kHz !

Fig. 11 shows overall power dissipation as a function of chip area for MOSFETs and IGBTs; the operating conditions are

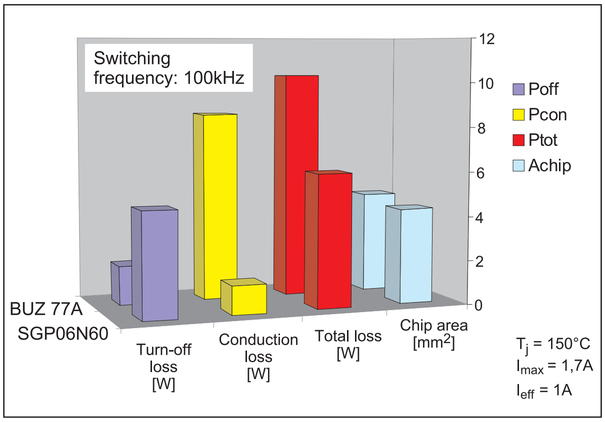

Fig. 8: Power dissipation comparison between a standard MOSFET and an S-IGBT of identical chip area in a switch mode power supply application at 100 kHz switching frequency

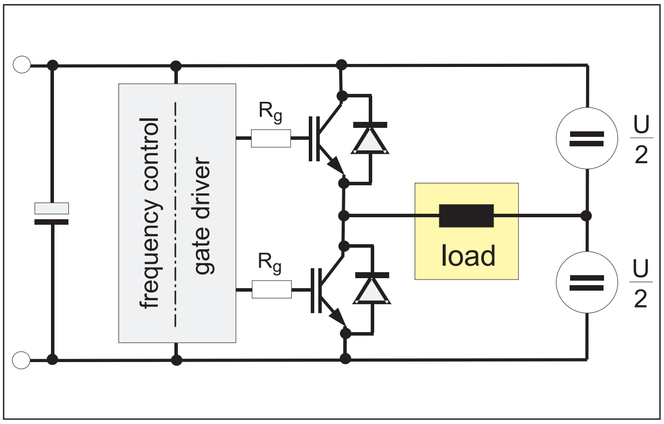

Fig. 9: Block diagram of the ZVS converter used for test purposes (U = 300V, switching frequency 100...500kHz)

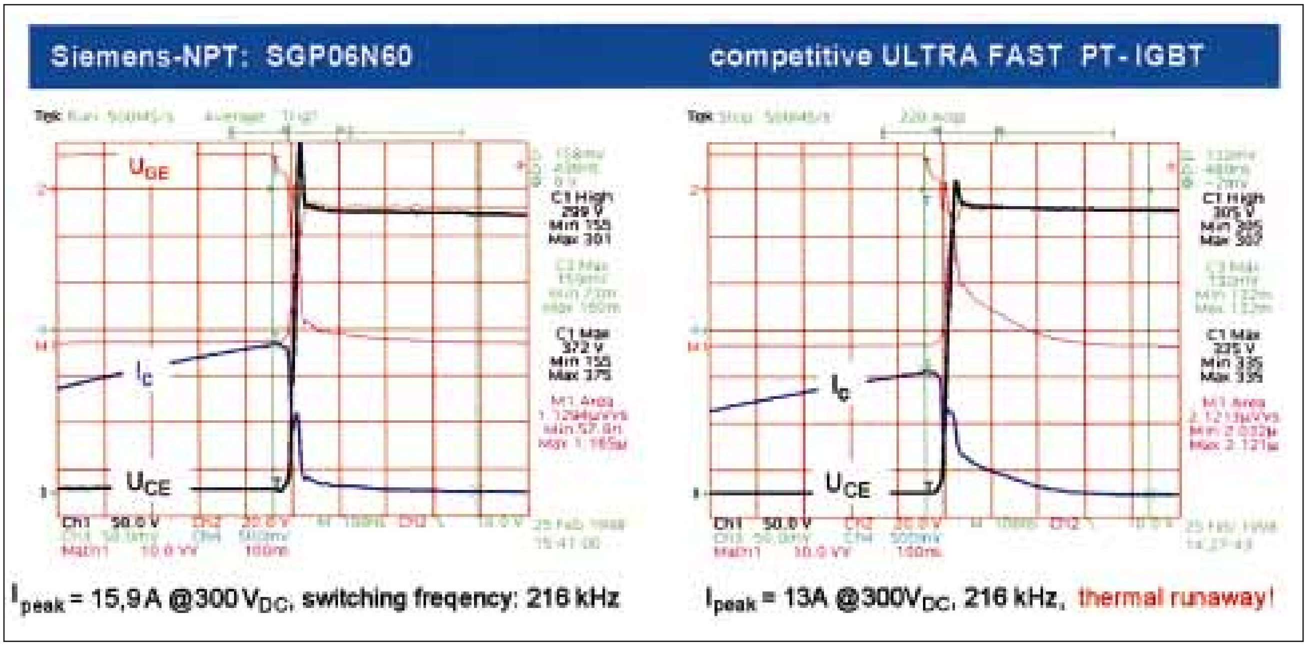

Fig. 10: Turn-off behavior of an NPT S-IGBT compared to one of the fastest PT-IGBTs (both types rated 6A at 100°C)

assumed to be as per the circuit in Fig. 9.

In the case of the MOSFET the expected response is obtained, with the losses initially reducing as the chip area increases and $R_{DS(on)}$ therefore decreases. Superimposed on this reduction is an increase in the dynamic losses at a given driver power, as the gate charge and therefore the switching times increase with the chip area. The lower the resistance at which the gate driver turns off the MOSFET, the further the increase in overall power dissipation can be shifted towards larger chip areas and the minimum power dissipation simultaneously lowered. Towards small chip areas, the characteristics end at the point where the thermal resistance of the device has become so high that the resultant power loss can no longer be dissipated.

Essentially the IGBT exhibits a similar response, although at high switching frequencies (>100 kHz), the branch of the curve determined by the on-state characteristics is barely achievable, as this would require power dissipation densities at which the chip would no longer be coolable. However, the essential difference from the MOSFET is that, because of the tail current, the dynamic turn-off losses can only be influenced to a very limited extent via the gate driver. In addition, it is generally the case that at a fixed current the tail losses increase with chip area.

For applications involving high switching frequencies, it flows directly from this that there is a lower limit to the power dissipation that can be achieved with an IGBT. Unlike MOSFETs, this minimum power dissipation is obtained at small chip areas and correspondingly high power dissipation densities. If the development objectives in terms of power dissipation can be fulfilled with an IGBT, the latter will generally constitute the most cost-effective solution, as it achieves its purpose with minimal chip area.

The comparison is particularly dramatic when the S-IGBTs are compared to the standard MOSFET technologies currently on the market. Under the conditions as per Fig. 11, for example, it would require a standard MOSFET with more than 30 mm² chip area – corresponding to an $R_{DS(on)}$ of about 0.5Ω – to achieve the power dissipation values of a 6A S-IGBT with just 5 mm² chip area. Because of the high crest factor (=peak value/r.m.s. value) of the switch current in the circuit in Fig. 9, the chip area relationship is even more striking here than in Fig. 6.

References

T. Laska, M. Matschitsch, W. Scholz: Ultrathin Wafer Technology for a NEW 600V-NPT-IGBT, ISPSD Weimar, May 26-29, 1997

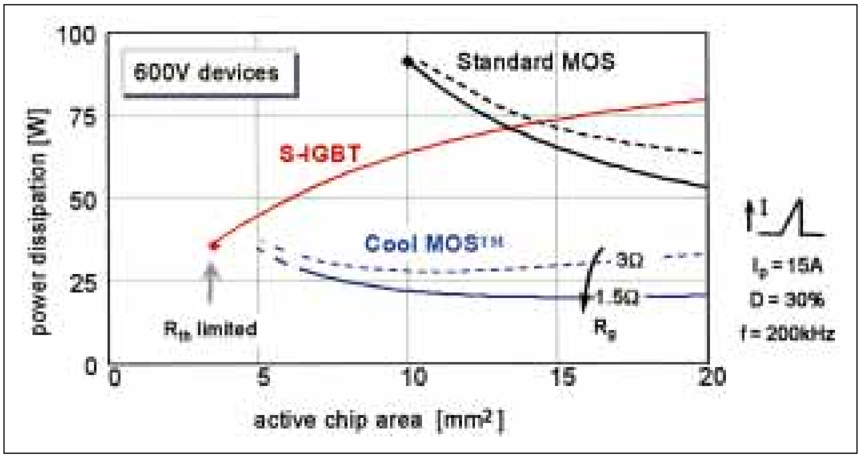

Fig. 11: Power dissipation as a function of chip area at 200 kHz switching frequency