SIMPLE FILTER DESIGN PROCEDURE FOR VOLTAGE FED SPACE VECTOR MODULATED CONVERTERS

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Abstract – **Space Vector Modulation (SVM) is widely used in industrial drives applications, and due its flexibility for the selection of the switching sequences as well as its suitability for digital implementation it is rapidly gaining favour in other applications such uninterruptible power supplies, force commutated rectifiers and active filters. In this context, this paper presents simple filter design procedure for different voltage fed space vector modulated (SVM) converters. The proposed design procedure is applied to six basic converters including single-phase and three-phase voltage fed rectifiers and inverters. Although, the normalized curves used in the design have been derived for a given symmetric switching sequence, it can be easily extended to other switching sequences. The paper describes in detail the proposed filter design procedure, including the supporting hypothesis and simplifications as well as a brief description of the SVM for converters considered. Aiming demonstrate the validity of the proposed design procedure, experimental results are also included.**

KEYWORDS

Space vector modulation, filter design, distortion factors, PWM voltage-fed converters.

I. INTRODUCTION

Voltage-fed converters have been used to synthesize AC voltage or current waveforms in several applications, such as uninterruptible power supplies (UPS's), motor drives and active filters. As a result, a number of converters topologies have been developed ranging from single-phase half-bridge to three-phase four-leg converters. In order to synthesize the desired voltage(s)/currents(s), several modulation strategies, differing in concept and performance have been developed [1-3]. The pulse width modulation (PWM) technique has the attractive characteristic of establishing the harmonic spectral components associated to the modulation at high frequencies, allowing the use of small filters to attenuate them [2]. In order to obtain optimized characteristics, different PWM schemes have been proposed, as the carrier-modulated sine PWM, the pre-calculated PWM and the space vector modulation [3-5]. The SVM has been receiving special attention since last decade because it allows to reduce the commutation losses and/or the harmonic content of output waveforms, and to obtain higher amplitude modulation indexes if compared with conventional PWM techniques [6,7]. Moreover, space vector modulation can be easily implemented in digital processors [8-10]. However, there is not reported systematic design procedure for the filter with space vector modulation converters such as for pulse-width modulation converters [11,12].

This paper presents a simple and systematic design procedure for the input/output filters for different voltage-fed space vector modulated converters. The proposed methodology is based on the concepts of distortion factors [3] that are now applied for SVM converters. The proposed design procedure is based on normalized design curves related to the switching sequences. Although the normalized design curves used in the design have been given for a symmetric switching sequence, it provides the basis for its extension to the other switching sequences.

The remainder of this paper is organized as follows. Section II presents in detail the principles of the proposed methodology, including the supporting hypothesis and simplifications. Section III gives a brief description of the SVM for the six analyzed topologies. Section IV validates the procedure experimentally.

II. FILTERS DESIGN PROCEDURE FOR SVM VOLTAGE-FED CONVERTERS

The proposed design procedure for the filters parameters is demonstrated in this section. First, the following assumptions about the space-vector modulated converters are made:

(i) The switches of the converter are ideal, and the switches of the same leg are controlled complementarily. As a result the voltage(s) that is (are) fed to filter is (are) determined by state of conduction of the switches and the DC bus voltage;

(ii) It is considered that the output voltage space is divided into regions, where for each region the switching sequence is defined a priori;

(iii) The command vector is regularly updated at a fixed frequency, which is considered be equal to the sample frequency. Here it is defined the normalized sampling frequency as $m_s=f_s/f_1$, where f_s is the sampling frequency and f_1 is the fundamental frequency.

The normalized sampling frequency (m_s) is independent of the number of commutations in a sampling period. This is a distinct concept if compared with the modulating frequency ratio (m_f) that in often used in conventional PWM modulated converters [1]. Therefore, in SVM converters, the switching frequency depends of the switching sequences adopted as well as on the normalized sampling frequency m_s. Aiming to illustrate this statement, it is presented in the Fig.1 two distinct SVM switching sequences with different number of commutations per sampling period for a "sector" of the single-phase full-bridge converter. This figure shows the patterns produced by the each leg. Performing the spectral

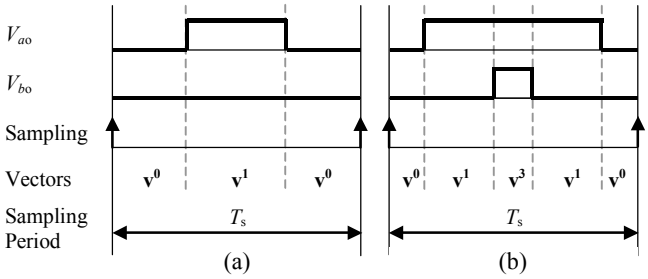

Fig. 1. Leg voltages, sampling instants and switching vectors in a given "sector" for two distinct switching sequences in a SVM single-phase full-bridge converter. (a) Switching sequence $\mathbf{v}^0\mathbf{v}^1\mathbf{v}^0$; (b) Switching sequence $\mathbf{v}^0\mathbf{v}^1\mathbf{v}^3\mathbf{v}^1\mathbf{v}^0$.

analysis of v_{ab} for a complete cycle of the modulating sinusoidal waveform for the two switching sequences, it is found out that the harmonics spectrum for both sequences are distinct, although they have same sampling frequency. The Fig. 2 shows the spectra for these switching sequences with m_s=64, where it can be seen that the first group of harmonics appears around the 64-th and 128-th harmonic, respectively.

The following subsections describe the design procedure for the first and second-order filters for the single-phase full-bridge converters, including the supporting hypothesis and simplifications. Then, it is depicted how to extend the described procedures to the others topologies.

1) Design of second-order filters for single-phase full-bridge converters: Fig.5b shows the power circuit of the single-phase full-bridge converter. It is considered that this converter is connected to the second-order output filter shown in the Fig.5c, and it is assumed that the design objective is to determine the corner frequency of the filter in order to obtain the given total harmonic distortion (*THD*) in the output voltage, where the THD_v is defined by

$$THD_v = \frac{1}{V_o(1)}\left(\sum_{n=2}^{\infty}\left[V_o(n)\right]^2\right)^{1/2}, \qquad (1)$$

n is the order of the harmonic, and $V_o(n)$ is the peak value of the n-th harmonic. Note that the voltage V_o can be expressed as a function of the inverter output voltage V_{ab}, that is

$$V_o(s) = G(s)V_{ab}(s) \qquad (2)$$

where $G(s)$ is a transfer function from the inverter output to the filter output, which in this case is given by

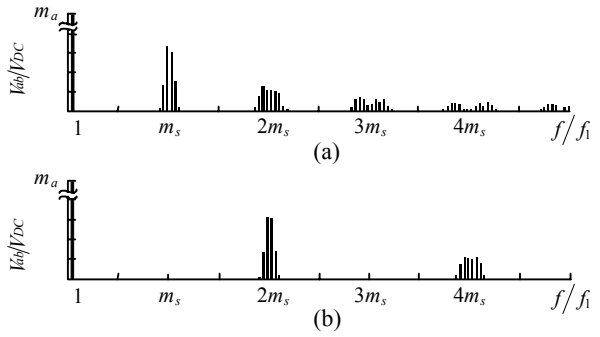

Fig. 2. Normalized frequency spectrum of v_{ab} for two different switching sequences in the single-phase full-bridge SVM converter modulated by a sinusoidal waveform with m_a=0.8, m_s=64. (a) Switching sequence $\mathbf{v}^0\mathbf{v}^1\mathbf{v}^0$; (b) Switching sequence $\mathbf{v}^0\mathbf{v}^1\mathbf{v}^3\mathbf{v}^1\mathbf{v}^0$.

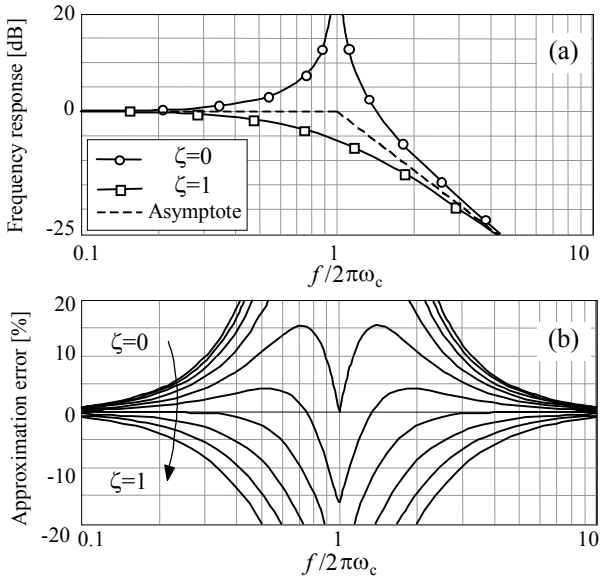

Fig. 3. (a) Normalized frequency response of $G(s)$ for ζ=0 and ζ=1 and the asymptote approximation for $G(s)$. (b) Error between the frequency response of $G(s)$ for $0\leq\zeta\leq1$ and it asymptote approximation, for $0.1\omega_c \leq \omega \leq 10\omega_c$.

$$G(s) = \frac{1}{s^2/\omega_c^2 + 2\zeta s/\omega_c + 1} \qquad (3)$$

where $\omega_c=2\pi f_c$ and ζ is the damping ratio.

The frequency response of $G(s)$ depends on the load. Fig. 3.a shows the frequency response of $G(s)$ and its asymptote approximation for different damping ratios (ζ=0 and ζ=1). It is worth mentioning, that the purpose of the filter is to attenuate the high order harmonics generated by the modulation. As a result, the corner frequency of the filter ω_c is usually smaller than the lowest high order harmonics generated by the SVM. Therefore, in the high order harmonics frequencies range, the frequency response of $G(s)$ can be approximated by a high frequency asymptote. For frequencies higher than $5\omega_c$ the error between the frequency response of $G(s)$ and its approximated frequency response is smaller then 5%, as seen in Fig.3b. It is also shown in Fig. 3.b shows this error in the low frequency range. This error is smaller then 1% for frequencies smaller then $0.1\omega_c$.

Assuming the $\omega_1\leq0.1\omega_c$ and that the SVM do not generate low order harmonics in the frequency band between $0.1\omega_c$ to $5\omega_c$. Then the frequency response of $G(s)$ can be expressed as:

$$\left|G(j\omega)\right| \approx \begin{cases} 1, & \text{for } \omega \leq 0.1\omega_c \\ \dfrac{\omega_c^2}{\omega^2}, & \text{for } \omega \geq 5\omega_c \end{cases} \qquad (4)$$

As a result the n-th order output voltage harmonic component can be written as

$$V_o(n) \approx \begin{cases} V_{ab}(1) & \text{, for } n = 1 \\ \left(\dfrac{\omega_c}{n\omega_1}\right)^2 V_{ab}(n) & \text{, for } n \neq 1 \end{cases} \qquad (5)$$

and the THD_v expression can be rewritten using (5) into (1) yields

$$THD_v = \frac{1}{V_{ab}(1)}\left(\sum_{n=2}^{\infty}\left[\left(\frac{\omega_c}{n\,\omega_1}\right)^2 V_{ab}(k)\right]^2\right)^{1/2} \tag{6}$$

Once the high order harmonics components of V_o with significant magnitude are in the side bands around the multiples (and submultiples) of the sampling frequency, for instance as shows the Fig. 2, (6) can be rewritten as,

$$THD_v = \frac{1}{V_{ab}(1)}\left(\sum_{k=a_1 m_s - b_1}^{a_1 m_s + b_1}\left[\left(\frac{\omega_c}{k\omega_1}\right)^2 V_{ab}(k)\right]^2 + \sum_{k=a_2 m_s - b_2}^{a_2 m_s + b_2}\left[\left(\frac{\omega_c}{k\omega_1}\right)^2 V_{ab}(k)\right]^2 + \cdots\right)^{1/2} \tag{7}$$

where a_1, a_2, ... are the relative spectral positions of the high order harmonics groups m of the spectrum of V_o. For example, in the presented topology, for the switching sequence $\mathbf{v}^0$-$\mathbf{v}^1$-$\mathbf{v}^0$, a_1=1, a_2=2,... , and for $\mathbf{v}^0$-$\mathbf{v}^1$-$\mathbf{v}^3$-$\mathbf{v}^1$-$\mathbf{v}^0$, a_1=2, a_2=4,... . On the other hand, b_1, b_2,... delimit the width of the side bands around $a_1 m_s$, $a_2 m_s$,…, respectively, where the harmonic components of V_o have a significant magnitude, for instance, greater than 1% of $V_o(1).$

Assuming that $a_1 m_s$, $a_2 m_s$, … are sufficiently large, the following approximations are valid,

$$\begin{aligned} &a_1 m_s - b_1 \approx a_1 m_s + b_1 \approx a_1 m_s, \\ &a_2 m_s - b_2 \approx a_2 m_s + b_2 \approx a_2 m_s, \ \cdots \end{aligned} \tag{8}$$

As a result (5) can be simplified as follows

$$THD_v = \left(\frac{\omega_c}{\omega_1}\right)^2 \frac{1}{m_s^2}\frac{1}{V_{ab}(1)}\left(\sum_{k=a_1 m_s - b_1}^{a_1 m_s + b_1}\left[\frac{V_{ab}(k)}{a_1^{\,2}}\right]^2 + \sum_{k=a_2 m_s - b_2}^{a_2 m_s + b_2}\left[\frac{V_{ab}(k)}{a_2^{\,2}}\right]^2 + \cdots\right)^{1/2} \tag{9}$$

In order to obtain an expression for the THD_v independent of the V_{DC}, the following normalizations are made: $V_{ab}^*(k) = V_{ab}(k)/V_{DC}$ and, $V_{ab}^*(1) = m_a = V_{ab}(1)/V_{DC}$. Hence, the equation (9) can be rewritten as

$$THD_v = \left(\frac{\omega_c}{\omega_1}\right)^2 \frac{1}{m_s^2}\frac{1}{m_a} nDF_2 \tag{10}$$

where

$$nDF_2 = \left(\sum_{k=a_1 m_s - b_1}^{a_1 m_s + b_1}\left[\frac{V_{ab}^*(k)}{a_1^{\,2}}\right]^2 + \sum_{k=a_2 m_s - b_2}^{a_2 m_s + b_2}\left[\frac{V_{ab}^*(k)}{a_2^{\,2}}\right]^2 + \cdots\right)^{1/2} \tag{11}$$

Aiming to demonstrate the validity of the simplifications carried out, Fig.4 shows several curves for nDF_2. These plots were obtained for a symmetric switching sequences for the full-bridge inverter with different m_s. Each curve is multiplied by it m_s^2 aiming to demonstrate that the errors due to the normalization are small for $m_s > 32$.

In order to simplify the design an abacus of nDF_2 is given in the Fig.12 for the sequence presented in the Table IV. Therefore, the corner frequency of the filter can be directly obtained from (10). The values of L and C can be determined from ω_c, by selecting one of them and calculating the other.

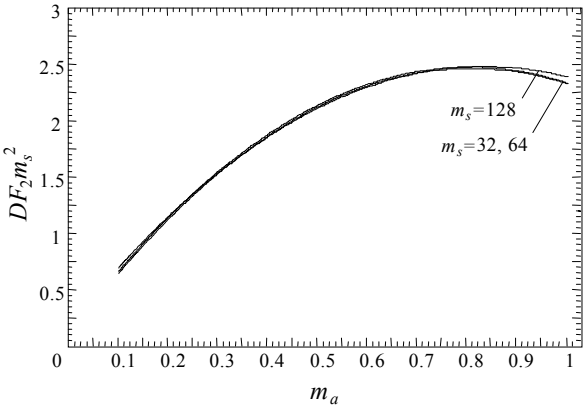

Fig. 4. Normalized distortion factor $nDF_2\ m_s^2$. Full bridge inverter with a symmetric SVM for m_s = 32, 64, 128.

2) Design of first-order filters for single-phase full-bridge converters: Let us consider the single-phase full-bridge converter is operating as controlled rectifier with a first-order input filter, which is shown in the Fig.5d. It is assumed that the design objective is to determine the inductance of the filter in order to obtain the given total harmonic distortion (*THD*) of the input current, where the THD_i is defined as

$$THD_i = \frac{1}{I_{in}(1)}\left(\sum_{n=2}^{\infty}\left[I_{in}(n)\right]^2\right)^{1/2} \tag{12}$$

and $I_{in}(n)$ is the peak value of the n-th harmonic component of i_{in} and $I_{in}(1)$ is the peak value of the fundamental component. The input current i_{in} can be expressed as a function of the inverter output voltage v_{ab} that is:

$$I_{in}(s) = G(s)V_{ab}(s) \tag{13}$$

where $G(s)$ in this case is given by

$$G(s) = 1/sL \tag{14}$$

Hence,

$$\left|G(j\omega)\right| = \left|\frac{I_{in}(j\omega)}{V_{ab}(j\omega)}\right| = \frac{1}{\omega L} = \frac{1}{n\,\omega_1 L} = \frac{1}{n\,X_L} \tag{15}$$

where $X_L = \omega_1 L$. It can be observed in (14) there is no difference between the asymptote approximation and the frequency response of the filter.

Therefore, by substituting (14) into (13) and assuming the same hypothesis made for (7) and (8), yields

$$THD_i = \frac{1}{X_L I_{in}(1)}\frac{1}{m_s}\left(\sum_{k=a_1 m_s - b_1}^{a_1 m_s + b_1}\left[\frac{V_{ab}(k)}{a_1}\right]^2 + \sum_{k=a_2 m_s - b_2}^{a_2 m_s + b_2}\left[\frac{V_{ab}(k)}{a_2}\right]^2 + \cdots\right)^{1/2} \tag{16}$$

Normalizing $V_{ab}(k)$ in relation to the DC bus, results in:

$$THD_i = \frac{V_{DC}}{X_L I_{in}(1)}\frac{1}{m_s} nDF_1 \tag{17}$$

where

$$nDF_1 = \left(\sum_{k=a_1 m_s - b_1}^{a_1 m_s + b_1}\left[\frac{V_{ab}^*(k)}{a_1}\right]^2 + \sum_{k=a_2 m_s - b_2}^{a_2 m_s + b_2}\left[\frac{V_{ab}^*(k)}{a_2}\right]^2 + \cdots\right)^{1/2} \tag{18}$$

In order to simplify the design the factor nDF_1 can be derived a priori. An abacus of nDF_1 in function of the modulation amplitude ratio (m_a) is given in the Fig.11, for the sequence presented in the Table IV. As a result, the value of the inductor for the filter can be directly determined from (17).

3) Extending the filter design procedure to others converters topologies: The proposed filter design procedure can be extended to others topologies by modifying adequately the expressions for THD_i and THD_v. The half-bridge and full-bridge converters have a similar filter structure and similar *THD* formulations. However, three-phase filters are MIMO and can contain coupled dynamics. In these cases, each output of the filter is related to a set of voltages generated by the legs of the converter. So, in order to obtain equations of the *THD* for the three-phase converters similar to (10) and (16), it is necessary to obtain the equivalent SISO transfer functions for $\mathbf{G}(s)$.

In order to demonstrate how the dynamic decoupling is achieved, let us considered the three-phase three-wire converters with a first-order output filter. The matrix transfer function for this converter is expressed as:

$$\mathbf{y}(s)=\mathbf{G}(s)\mathbf{V}(s)$$
$$\begin{bmatrix} I_a(s) \\ I_b(s) \end{bmatrix}=\begin{bmatrix} 2/(3sL) & 1/(3sL) \\ -1/(3sL) & 1/(3sL) \end{bmatrix}\begin{bmatrix} V_{ab}(s) \\ V_{bc}(s) \end{bmatrix} \quad (19)$$

It is assumed that the structure and parameters of the filter are symmetric. In this way, it is ensured that every element of $\mathbf{G}(s)$ present an similar s-domain rational polynomial function, as can be seen in (19), where the differences among the entries are their gains. As a result, the matrix transfer function $\mathbf{G}(s)$ can be expressed as:

$$\mathbf{y}(s)=g(s)\mathbf{G}_c\mathbf{V}(s)$$
$$=\frac{1}{3Ls}\begin{bmatrix} 2 & 1 \\ -1 & 1 \end{bmatrix}\begin{bmatrix} V_{ab}(s) \\ V_{bc}(s) \end{bmatrix} \quad (20)$$

By rewriting (20), it possible to obtain on equivalent decoupled transfer function, that is:

$$\mathbf{y}(s)=g(s)\mathbf{G}_c\mathbf{V}(s)=\left(1/3Ls\right)\mathbf{V}_{eq}(s) \quad (21)$$

where

$$\mathbf{V}_{eq}(s)=\mathbf{G}_c\mathbf{V}(s)=\begin{bmatrix} 2 & 1 \\ -1 & 1 \end{bmatrix}\begin{bmatrix} V_{ab}(s) \\ V_{bc}(s) \end{bmatrix}=\begin{bmatrix} V_{e1,1}(s) \\ V_{e1,2}(s) \end{bmatrix} \quad (22)$$

So the matrix transfer function can be rewritten as equivalent SISO transfer functions. For the considered converter, the equivalent SISO transfer functions of (19) are expressed as

$$\begin{aligned} i_a(s)&=g(s)V_{e1,1}(s) \\ i_b(s)&=g(s)V_{e1,2}(s) \end{aligned} \quad (23)$$

As $g(s)$ in (23) are similar to $G(s)$ in (14), the determination of the THD_i for each current in the considered converter can be performed using the same procedure described in Section II.2. For instance, substituting (14) by $g(s)$ and V_{ab} by $V_{e1,1}$ in (16), it is obtained in (17) the THD_i for i_a.

This methodology for the dynamic decoupling can be directly applied to the others first-order and second-order filters. Where for, the second-order filters it is required the same considerations for $\mathbf{G}(s)$ as earlier described for $G(s)$ in the Section II.1.

So it is possible to write generic equations for the *THD* of all elements of $\mathbf{y}(s)$. These equations are written in function of the normalized modulation amplitude ratio m, $0\le m\le 1$. The relation between m and m_a is give as: $m = m_a / g$, where g is defined as the maximum possible line-to-line voltage (first four topologies in Table I) or phase voltage (last two topologies in Table I), that can be generated by converter in relation to the DC bus. The generic equations of the *THD* are given as

$$THD_{v,j}=\frac{1}{g}\frac{1}{c}\left(\frac{\omega_c}{\omega_1}\right)^2\frac{1}{m_s^2}\frac{1}{m}nDF_{2,j} \quad (24)$$

$$THD_{i,j}=\frac{1}{c}\frac{V_{DC}}{X_L I_a(1)}\frac{1}{m_s}nDF_{1,j} \quad (25)$$

where exception

$$nDF_{2,j}=\left(\sum_{k=a_1m_s-b_1}^{a_1m_s+b_1}\left[\frac{V_{e2,j}^*(k)}{a_1^{\,2}}\right]^2+\sum_{k=a_2m_s-b_2}^{a_2m_s+b_2}\left[\frac{V_{e2,j}^*(k)}{a_2^{\,2}}\right]^2+\cdots\right)^{1/2} \quad (26)$$

$$nDF_{1,j}=g\left(\sum_{k=a_1m_s-b_1}^{a_1m_s+b_1}\left[\frac{V_{e1,j}^*(k)}{a_1}\right]^2+\sum_{k=a_2m_s-b_2}^{a_2m_s+b_2}\left[\frac{V_{e1,j}^*(k)}{a_2}\right]^2+\cdots\right)^{1/2} \quad (27)$$

j is the index of the element of $\mathbf{y}(s)$, c is a parameter associated to the $g(s)$ of each topology and $V_{e1,j}^*(k)=V_{e1,j}(k)/gV_{DC}$, $V_{e2,j}^*(k)=V_{e2,j}(k)/gV_{DC}$.

In those topologies were the PWM patterns in each phase are identical (except for a shifting in time), the resulting *THD* in all elements of $\mathbf{y}(s)$ are equal. For the converters described in this paper, only the three-phase three-wire two-leg does not have this property. So, in order to obtain a single abacus for the selected switching sequence, the curves of nDF_1 and nDF_2 were plotted to ensure that in all outputs the *THD* is equal or smaller than the specified.

The Table I present the values for c, g, m, $V_{e1,1}$ and $V_{e2,1}$ for the six basic voltage-fed converters topologies considered. It worth to emphasize that the normalized design curves provided for the three-phase three-wire converters are related to line-to-line voltages, while the analysis for the three-phase four-wire converters are related to phase voltages. As a

TABLE I
Parameters for the calculation of THD_i and THD_v in the six basic converters topologies

Inverter topology	m	c	g	$V_{e1,1}$	$V_{e2,1}$
Single-phase half-bridge	$2V_{ab}/V_{DC}$	1	1/2	V_{ab}	V_{ab}
Single-phase full-bridge	V_{ab}/V_{DC}	1	1	V_{ab}	V_{ab}
Three-phase three-wire two-leg	$\sqrt{6}\,V_{ab}/V_{DC}$	3	$1/\sqrt{6}$	$2V_{ab}+V_{bc}$	V_{ab}
Three-phase three-wire three-leg	V_{ab}/V_{DC}	3	1	$2V_{ab}+V_{bc}$	V_{ab}
Three-phase four-wire three-leg	$2\,V_{ao}/V_{DC}$	4	1/2	$3V_{ao}-V_{bo}-V_{co}$	$3V_{ao}-V_{bo}-V_{co}-V_{no}$
Three-phase four-wire four-leg	$\sqrt{3}\,V_{ao}/V_{DC}$	4	$1/\sqrt{3}$	$3V_{ao}-V_{bo}-V_{co}$	$3V_{ao}-V_{bo}-V_{co}-V_{no}$

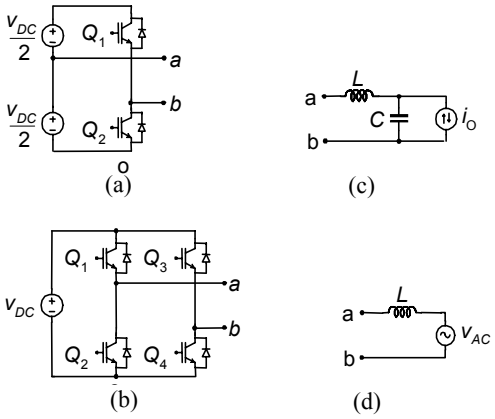

Fig.5. Single-phase converters and their input/output filters: (a) half-bridge topology; (b) full-bridge topology; (c) second-order filter; (d) first-order filter.

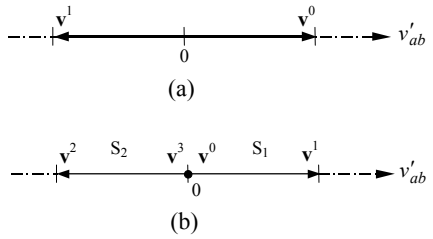

Fig.6. Output voltage spaces of single-phase converters: (a) half-bridge topology; (b) full-bridge topology.

result, the *THD* and the normalized modulation amplitude ratio (*m*) are also associated to line-to-line voltage for the former and phase voltages for the later.

III. SVM FOR THE SIX BASIC VOLTAGE-FED CONVERTERS

This section presents the SVM for the six-basic topologies of voltage-fed converters. Each topology can be characterized by its possible switching vectors and it input/output voltage space. The boundary and separation "planes" and the decomposition matrices for each topology where omitted for most of the topologies, since they have been presented in [5]. Only the three-phase two-leg converter has the boundary and separation "planes" presented here (in appendix), once it has not been presented in [5].

In the following subsections are presented the possible switching vectors and a selected switching sequence for each topology. In addition, the linear transformations applied to the switching vectors in order to simplify the analysis of the output voltage spaces are described. Furthermore, they also include the switching sequences selected for the plotting of normalized design curves of nDF_1 and nDF_2. The abaci of nDF_1 and nDF_2 are given in the Fig.11 and Fig.12, respectively.

1) Single-phase half-bridge voltage-fed converter: This converter, shown in the Fig.5(a), presents two possible switching vectors, as shown in Table II. The output voltage space is of dimension one, with a single sector, as shown in Fig.6(a). The only switching sequence for this converter is presented in Table IV.

TABLE II
Possible switching vectors of the single-phase half-bridge converter

Q_1	v'_{ao}	v'_{bo}	v'_{ab}	Vectors
0	1/2	0	1/2	$\mathbf{v}^0$
1	1/2	1	-1/2	$\mathbf{v}^1$

TABLE III
Possible switching vectors of the single-phase full-bridge converter

Q_1	Q_3	v'_{ao}	v'_{bo}	v'_{ab}	Vectors
0	0	0	0	0	$\mathbf{v}^0$
1	0	1	0	1	$\mathbf{v}^1$
0	1	0	1	-1	$\mathbf{v}^2$
1	1	1	1	0	$\mathbf{v}^3$

TABLE IV
Switching sequences for the single-phase converters

Sector	Half-bridge converter	Full-bridge converter
1	$\mathbf{v}^1$-$\mathbf{v}^2$	$\mathbf{v}^0$-$\mathbf{v}^1$-$\mathbf{v}^0$
2	-	$\mathbf{v}^0$-$\mathbf{v}^2$-$\mathbf{v}^0$

2) Single-phase full-bridge voltage-fed converter: This converter is shown in the Fig.5(b). It presents four possible switching vectors, as shown in Table III. Its output voltage space is of dimension one, with two distinct "sectors", as shown in Fig.6(b). The selected switching sequence for the plotting of normalized design curves is presented in Table IV, whose PWM pattern is shown in the Fig.1(a).

3) Three-phase two-legs three-wire voltage-fed converter: This converter, shown in the Fig.7(a), presents four possible switching vectors as can be seen in the Table V. As the output voltage space is of dimension two, in order to simplify the analysis, it have been applied abc to $\chi\delta$ transformation ($\Re_3 \rightarrow \Re_2$), which is given by (28). The resulting output voltage space is illustrated in Fig.8(a), where it is possible to be identified four distinct "sectors". The selected switching sequence for the plotting of nDF_1 and nDF_2 is given in Table VII.

$$\mathbf{T}_{\chi\delta} = \begin{bmatrix} \sqrt{2}/2 & -\sqrt{2}/2 & 0 \\ \sqrt{6}/6 & \sqrt{6}/6 & -\sqrt{3}/2 \end{bmatrix} \tag{28}$$

4) Three-phase three-legs three-wire voltage-fed converter This converter, shown in the Fig.7(b), presents eight possible switching vectors as can be seen in the Table VI. The output voltage space is of dimension two, as illustrated in Fig.8(b). For this figure it have been used the abc to $\alpha\beta$ transformation ($\Re_3 \rightarrow \Re_2$) given by (29). The output voltage space has six distinct "sectors", that are also illustrated in Fig.8(b). In addition, the selected switching sequence to derive the normalized design curves of the Fig.11 and Fig.12 is presented in Table VII.

$$\mathbf{T}_{\alpha\beta} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix} \tag{29}$$

5) Three-phase three-legs four-wire voltage-fed converter: This converter, shown in the Fig.9(a), has eight possible

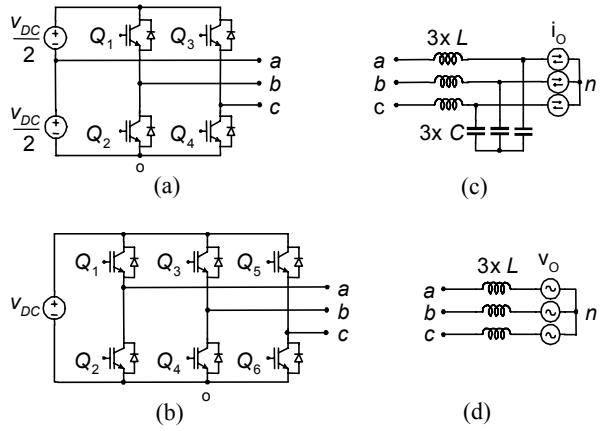

Fig.7. Three-phase three-wire converters and their input/output filters: (a) two-leg topology; (b) three-leg topology; (c) second-order filter; (d) first-order filter.

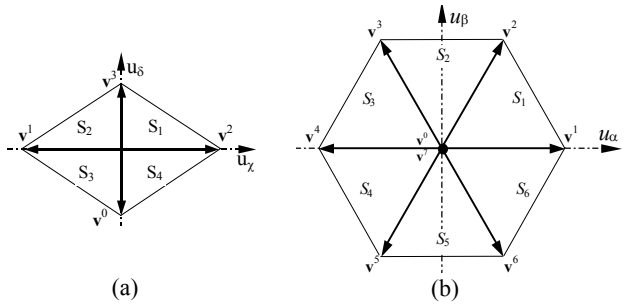

Fig.8. Output voltage spaces of the three-phase three-wire converters: (a) two-leg topology in χδ coordinates; (b) three-leg topology in αβ coordinates.

switching vectors as can be seen in the Table VIII. The resulting output voltage space is of dimension three, as can be seen in Fig.10(a). As this converter is usually analyzed in a 0αβ coordinates, the abc to 0αβ transformation ($\Re_3 \rightarrow \Re_3$) given by (30) has been applied to its switching vectors. The resulting output voltage space has six distinct sectors (tetrahedrons), as shows the Fig.10(a). The selected switching sequence for design in Table X.

$$\mathbf{T}_{0\alpha\beta} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1/\sqrt{2} & 1/\sqrt{2} & 1/\sqrt{2} \\ 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix} \qquad (30)$$

6) Three-phase four-legs four-wire voltage-fed converters: This converter, shown in the Fig.9(b), presents sixteen possible switching vectors as can be seen in the Table IX. The resulting output voltage space is of dimension three, as can be seen in Fig.10(b). It has been applied the abc to 0αβ transformation ($\Re_3 \rightarrow \Re_3$) to its switching vectors. The output voltage space has twenty-four distinct sectors (tetrahedrons). The selected switching sequence for the given curves is presented in Table X.

IV. EXPERIMENTAL EVALUATION OF THE FILTER DESIGN PROCEDURE

In this section experimental results of the proposed design procedure are presented. In order to exemplify the procedure second-order low-pass output filters for three-phase four-legs four-wire inverter has been designed. The designed filters

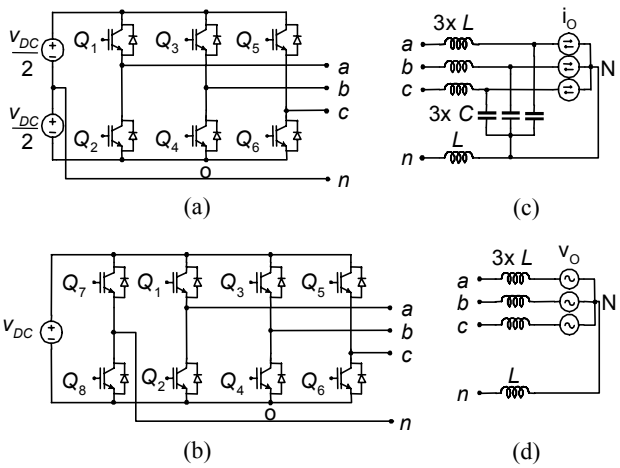

Fig. 9. Three-phase four-wire converters and their input/output filters: (a) three-leg topology; (b) four-leg topology; (c) second-order filter; (d) first-order filter.

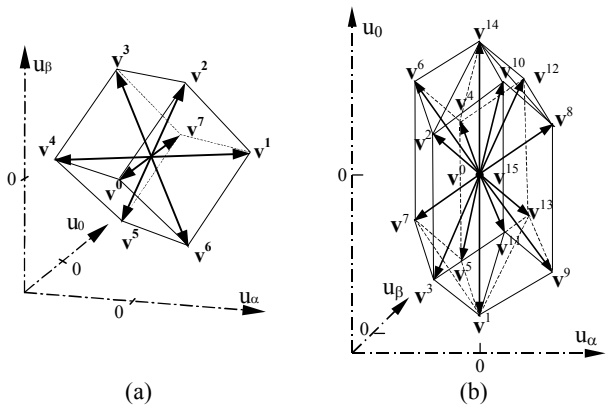

Fig.10. Output voltage space of the three-phase four-wire converters in 0αβ coordinates: (a) Three-leg topology; (b) Four-leg topology.

were experimentally evaluated using a 15 kVA four-leg voltage-source inverter with a V_{DC} = 350V DC bus, where the SVM were generated by a TMS320F241 DSP controller.

The following specifications have been considered for the design: f_1=60Hz, THD_v=2%, m=1 (m_a=0.577), f_s=5kHz and the switching sequence given by Table X. From this specifications the corner frequency of this filter was determined using (24), where $m_s = f_s / f_1$=83.33, c=4 (see Table I) and where the nDF_2 distortion factor was obtained from the abacus of Fig.11. In this case, nDF_2=0.66, that applied in (24) results in ω_c= 8305rad/s. An inductor of L=250μH has been chosen, and using the relation $\omega_c = 1/\sqrt{LC}$, the capacitor has been determined as C=58μF. A commercial value of 60μF has been selected. For this values of L and C, a THD_v=1.73% have been found from simulation. Then the THD_v in this filter was measured experimentally. The inverter was tested with the same given specifications at no-load, resulting in THD_v=1.14%.

The Table XI presents other results for different normalized modulation amplitude ratios, switching frequencies and filter parameters. It is seen a good agreement between of the THD_v calculated by the proposed design procedure and the THD_v obtained experimentally. These

TABLE V
Possible switching vectors of the three-phase two-leg three-wire converter

Q_1	Q_3	v'_{ab}	v'_{bc}	v'_{ca}	v'_{χ}	v'_{δ}	Vectors
0	0	1/2	0	-1/2	$-\sqrt{6}/6$	0	$\mathbf{v}^0$
0	1	1/2	-1	1/2	0	$-\sqrt{2}/2$	$\mathbf{v}^1$
1	0	-1/2	1	-1/2	0	$\sqrt{2}/2$	$\mathbf{v}^2$
1	1	-1/2	0	1/2	$\sqrt{6}/6$	0	$\mathbf{v}^3$

TABLE VI
Possible switching vectors of the three-phase three-leg three-wire converter

Q_1	Q_3	Q_5	v'_{ab}	v'_{bc}	v'_{ca}	v'_{α}	v'_{β}	Vectors
0	0	0	0	0	0	0	0	$\mathbf{v}^0$
0	0	1	0	-1	1	$\sqrt{2/3}$	0	$\mathbf{v}^1$
0	1	0	-1	1	0	$1/\sqrt{6}$	$1/\sqrt{2}$	$\mathbf{v}^2$
0	1	1	-1	0	1	$-1/\sqrt{6}$	$1/\sqrt{2}$	$\mathbf{v}^3$
1	0	0	1	0	-1	$-\sqrt{2/3}$	0	$\mathbf{v}^4$
1	0	1	1	-1	0	$-1/\sqrt{6}$	$-1/\sqrt{2}$	$\mathbf{v}^5$
1	1	0	0	1	-1	$1/\sqrt{6}$	$-1/\sqrt{2}$	$\mathbf{v}^6$
1	1	1	0	0	0	0	0	$\mathbf{v}^7$

TABLE VII
Switching sequences for three-phase three-wire converter

Sector	Two-leg converter	Three-leg converter
S_1	$\mathbf{v}^0$-$\mathbf{v}^2$-$\mathbf{v}^3$-$\mathbf{v}^2$-$\mathbf{v}^0$	$\mathbf{v}^0$-$\mathbf{v}^1$-$\mathbf{v}^2$-$\mathbf{v}^7$-$\mathbf{v}^2$-$\mathbf{v}^1$-$\mathbf{v}^0$
S_2	$\mathbf{v}^0$-$\mathbf{v}^1$-$\mathbf{v}^3$-$\mathbf{v}^1$-$\mathbf{v}^0$	$\mathbf{v}^0$-$\mathbf{v}^3$-$\mathbf{v}^2$-$\mathbf{v}^7$-$\mathbf{v}^2$-$\mathbf{v}^3$-$\mathbf{v}^0$
S_3	$\mathbf{v}^0$-$\mathbf{v}^1$-$\mathbf{v}^3$-$\mathbf{v}^1$-$\mathbf{v}^0$	$\mathbf{v}^0$-$\mathbf{v}^3$-$\mathbf{v}^4$-$\mathbf{v}^7$-$\mathbf{v}^4$-$\mathbf{v}^3$-$\mathbf{v}^0$
S_4	$\mathbf{v}^0$-$\mathbf{v}^2$-$\mathbf{v}^3$-$\mathbf{v}^2$-$\mathbf{v}^0$	$\mathbf{v}^0$-$\mathbf{v}^5$-$\mathbf{v}^4$-$\mathbf{v}^7$-$\mathbf{v}^4$-$\mathbf{v}^5$-$\mathbf{v}^0$
S_5	-	$\mathbf{v}^0$-$\mathbf{v}^5$-$\mathbf{v}^6$-$\mathbf{v}^7$-$\mathbf{v}^6$-$\mathbf{v}^5$-$\mathbf{v}^0$
S_6	-	$\mathbf{v}^0$-$\mathbf{v}^1$-$\mathbf{v}^6$-$\mathbf{v}^7$-$\mathbf{v}^6$-$\mathbf{v}^1$-$\mathbf{v}^0$

TABLE VIII
Possible switching vectors of the three-phase three-leg four-wire converter

Q_1	Q_3	Q_5	v'_{an}	v'_{bn}	v'_{cn}	v'_0	v'_{α}	v'_{β}	Vectors
0	0	0	–1/2	–1/2	–1/2	$-\sqrt{3}/2$	0	0	$\mathbf{v}^0$
1	0	0	1/2	–1/2	–1/2	$-\sqrt{3}/6$	$\sqrt{6}/3$	0	$\mathbf{v}^1$
1	1	0	1/2	1/2	–1/2	$\sqrt{3}/6$	$1/\sqrt{6}$	$\sqrt{2}/2$	$\mathbf{v}^2$
0	1	0	–1/2	1/2	–1/2	$-\sqrt{3}/6$	$-1/\sqrt{6}$	$\sqrt{2}/2$	$\mathbf{v}^3$
0	1	1	–1/2	1/2	1/2	$\sqrt{3}/6$	$-\sqrt{6}/3$	0	$\mathbf{v}^4$
0	0	1	–1/2	1/2	–1/2	$-\sqrt{3}/6$	$-1/\sqrt{6}$	$-\sqrt{2}/2$	$\mathbf{v}^5$
1	0	1	1/2	–1/2	1/2	$\sqrt{3}/6$	$1/\sqrt{6}$	$-\sqrt{2}/2$	$\mathbf{v}^6$
1	1	1	1/2	1/2	1/2	$\sqrt{3}/2$	0	0	$\mathbf{v}^7$

comparisons clearly demonstrate the validity of the proposed methodology.

V. CONCLUSIONS

This paper presents a filter design procedure for SVM voltage-fed converters. The supporting hypothesis and simplifications as well as a brief description of the SVM are also presented. It has been shown that the proposed procedure is straightforward and that it can be easily extended to others converters and others switching sequences. Finally, comparisons between theoretical and experimental results have been used to demonstrate the validity of the proposed methodology.

TABLE IX
Possible switching vectors of the three-phase four-wire four-leg converter

Q_1	Q_3	Q_5	Q_7	v'_{an}	v'_{bn}	v'_{cn}	v'_0	v'_{α}	v'_{β}	Vectors
0	0	0	0	0	0	0	0	0	0	$\mathbf{v}^0$
0	0	0	1	–1	–1	–1	0	0	$-\sqrt{3}$	$\mathbf{v}^1$
0	0	1	0	0	0	1	$-\sqrt{6}/6$	$-\sqrt{2}/2$	$\sqrt{3}/3$	$\mathbf{v}^2$
0	0	1	1	–1	–1	0	$-\sqrt{6}/6$	$-\sqrt{2}/2$	$-2\sqrt{3}/3$	$\mathbf{v}^3$
0	1	0	0	0	1	0	$-\sqrt{6}/6$	$\sqrt{2}/2$	$\sqrt{3}/3$	$\mathbf{v}^4$
0	1	0	1	–1	0	–1	$-\sqrt{6}/6$	$\sqrt{2}/2$	$-2\sqrt{3}/3$	$\mathbf{v}^5$
0	1	1	0	0	1	1	$-\sqrt{6}/3$	0	$2\sqrt{3}/3$	$\mathbf{v}^6$
0	1	1	1	–1	0	0	$-\sqrt{6}/3$	0	$-\sqrt{3}/3$	$\mathbf{v}^7$
1	0	0	0	1	0	0	$\sqrt{6}/3$	0	$\sqrt{3}/3$	$\mathbf{v}^8$
1	0	0	1	0	–1	–1	$\sqrt{6}/3$	0	$-2\sqrt{3}/3$	$\mathbf{v}^9$
1	0	1	0	1	0	1	$\sqrt{6}/6$	$-\sqrt{2}/2$	$2\sqrt{3}/3$	$\mathbf{v}^{10}$
1	0	1	1	0	–1	0	$\sqrt{6}/6$	$-\sqrt{2}/2$	$-\sqrt{3}/3$	$\mathbf{v}^{11}$
1	1	0	0	1	1	0	$\sqrt{6}/6$	$\sqrt{2}/2$	$2\sqrt{3}/3$	$\mathbf{v}^{12}$
1	1	0	1	0	0	–1	$\sqrt{6}/6$	$\sqrt{2}/2$	$\sqrt{3}/3$	$\mathbf{v}^{13}$
1	1	1	0	1	1	1	0	0	$\sqrt{3}$	$\mathbf{v}^{14}$
1	1	1	1	0	0	0	0	0	0	$\mathbf{v}^{15}$

TABLE X
Switching sequence for the three-phase four-wire converter

Tetrahedron	Three-leg four-wire converter	Four-leg four-wire converter
S_1	$\mathbf{v}^0$-$\mathbf{v}^1$-$\mathbf{v}^2$-$\mathbf{v}^7$-$\mathbf{v}^2$-$\mathbf{v}^1$-$\mathbf{v}^0$	$\mathbf{v}^0$-$\mathbf{v}^8$-$\mathbf{v}^{12}$- $\mathbf{v}^{14}$-$\mathbf{v}^{15}$-$\mathbf{v}^{14}$-$\mathbf{v}^{12}$-$\mathbf{v}^8$-$\mathbf{v}^0$
S_2	$\mathbf{v}^0$-$\mathbf{v}^3$-$\mathbf{v}^2$-$\mathbf{v}^7$-$\mathbf{v}^2$-$\mathbf{v}^3$-$\mathbf{v}^0$	$\mathbf{v}^0$-$\mathbf{v}^8$-$\mathbf{v}^{12}$-$\mathbf{v}^{13}$-$\mathbf{v}^{15}$-$\mathbf{v}^{13}$-$\mathbf{v}^{12}$-$\mathbf{v}^8$-$\mathbf{v}^0$
S_3	$\mathbf{v}^0$-$\mathbf{v}^3$-$\mathbf{v}^4$-$\mathbf{v}^7$-$\mathbf{v}^4$-$\mathbf{v}^3$-$\mathbf{v}^0$	$\mathbf{v}^0$-$\mathbf{v}^8$-$\mathbf{v}^9$-$\mathbf{v}^{13}$-$\mathbf{v}^{15}$-$\mathbf{v}^{13}$-$\mathbf{v}^9$-$\mathbf{v}^8$-$\mathbf{v}^0$
S_4	$\mathbf{v}^0$-$\mathbf{v}^5$-$\mathbf{v}^4$-$\mathbf{v}^7$-$\mathbf{v}^4$-$\mathbf{v}^5$-$\mathbf{v}^0$	$\mathbf{v}^0$-$\mathbf{v}^1$-$\mathbf{v}^9$-$\mathbf{v}^{13}$-$\mathbf{v}^{15}$-$\mathbf{v}^{13}$-$\mathbf{v}^9$-$\mathbf{v}^1$-$\mathbf{v}^0$
S_5	$\mathbf{v}^0$-$\mathbf{v}^5$-$\mathbf{v}^6$-$\mathbf{v}^7$-$\mathbf{v}^6$-$\mathbf{v}^5$-$\mathbf{v}^0$	$\mathbf{v}^0$-$\mathbf{v}^4$-$\mathbf{v}^{12}$-$\mathbf{v}^{14}$-$\mathbf{v}^{15}$-$\mathbf{v}^{14}$-$\mathbf{v}^{12}$-$\mathbf{v}^4$-$\mathbf{v}^0$
S_6	$\mathbf{v}^0$-$\mathbf{v}^1$-$\mathbf{v}^6$-$\mathbf{v}^7$-$\mathbf{v}^6$-$\mathbf{v}^1$-$\mathbf{v}^0$	$\mathbf{v}^0$-$\mathbf{v}^4$-$\mathbf{v}^{12}$-$\mathbf{v}^{13}$-$\mathbf{v}^{15}$-$\mathbf{v}^{13}$-$\mathbf{v}^{12}$-$\mathbf{v}^4$-$\mathbf{v}^0$
S_7	-	$\mathbf{v}^0$-$\mathbf{v}^4$-$\mathbf{v}^5$-$\mathbf{v}^{13}$-$\mathbf{v}^{15}$-$\mathbf{v}^{13}$-$\mathbf{v}^5$-$\mathbf{v}^4$-$\mathbf{v}^0$
S_8	-	$\mathbf{v}^0$-$\mathbf{v}^1$-$\mathbf{v}^5$-$\mathbf{v}^{13}$-$\mathbf{v}^{15}$-$\mathbf{v}^{13}$-$\mathbf{v}^5$-$\mathbf{v}^1$-$\mathbf{v}^0$
S_9	-	$\mathbf{v}^0$-$\mathbf{v}^4$-$\mathbf{v}^6$-$\mathbf{v}^{14}$-$\mathbf{v}^{15}$-$\mathbf{v}^{14}$-$\mathbf{v}^6$-$\mathbf{v}^4$-$\mathbf{v}^0$
S_{10}	-	$\mathbf{v}^0$-$\mathbf{v}^4$-$\mathbf{v}^6$-$\mathbf{v}^7$-$\mathbf{v}^{15}$-$\mathbf{v}^7$-$\mathbf{v}^6$-$\mathbf{v}^4$-$\mathbf{v}^0$
S_{11}	-	$\mathbf{v}^0$-$\mathbf{v}^4$-$\mathbf{v}^5$-$\mathbf{v}^7$-$\mathbf{v}^{15}$-$\mathbf{v}^7$-$\mathbf{v}^5$-$\mathbf{v}^4$-$\mathbf{v}^0$
S_{12}	-	$\mathbf{v}^0$-$\mathbf{v}^1$-$\mathbf{v}^5$-$\mathbf{v}^7$-$\mathbf{v}^{15}$-$\mathbf{v}^7$-$\mathbf{v}^5$-$\mathbf{v}^1$-$\mathbf{v}^0$
S_{13}	-	$\mathbf{v}^0$-$\mathbf{v}^2$-$\mathbf{v}^6$-$\mathbf{v}^{14}$-$\mathbf{v}^{15}$-$\mathbf{v}^{14}$-$\mathbf{v}^6$-$\mathbf{v}^2$-$\mathbf{v}^0$
S_{14}	-	$\mathbf{v}^0$-$\mathbf{v}^2$-$\mathbf{v}^6$-$\mathbf{v}^7$-$\mathbf{v}^{15}$-$\mathbf{v}^7$-$\mathbf{v}^6$-$\mathbf{v}^2$-$\mathbf{v}^0$
S_{15}	-	$\mathbf{v}^0$-$\mathbf{v}^2$-$\mathbf{v}^3$-$\mathbf{v}^7$-$\mathbf{v}^{15}$-$\mathbf{v}^7$-$\mathbf{v}^3$-$\mathbf{v}^2$-$\mathbf{v}^0$
S_{16}	-	$\mathbf{v}^0$-$\mathbf{v}^1$-$\mathbf{v}^3$-$\mathbf{v}^7$-$\mathbf{v}^{15}$-$\mathbf{v}^7$-$\mathbf{v}^3$-$\mathbf{v}^1$-$\mathbf{v}^0$
S_{17}	-	$\mathbf{v}^0$-$\mathbf{v}^2$-$\mathbf{v}^{10}$-$\mathbf{v}^{14}$-$\mathbf{v}^{15}$-$\mathbf{v}^{14}$-$\mathbf{v}^{10}$-$\mathbf{v}^2$-$\mathbf{v}^0$
S_{18}	-	$\mathbf{v}^0$-$\mathbf{v}^2$-$\mathbf{v}^{10}$-$\mathbf{v}^{11}$-$\mathbf{v}^{15}$-$\mathbf{v}^{11}$-$\mathbf{v}^{10}$-$\mathbf{v}^2$-$\mathbf{v}^0$
S_{19}	-	$\mathbf{v}^0$-$\mathbf{v}^2$-$\mathbf{v}^3$-$\mathbf{v}^{11}$-$\mathbf{v}^{15}$-$\mathbf{v}^{11}$-$\mathbf{v}^3$-$\mathbf{v}^2$-$\mathbf{v}^0$
S_{20}	-	$\mathbf{v}^0$-$\mathbf{v}^1$-$\mathbf{v}^3$-$\mathbf{v}^{11}$-$\mathbf{v}^{15}$-$\mathbf{v}^{11}$-$\mathbf{v}^3$-$\mathbf{v}^1$-$\mathbf{v}^0$
S_{21}	-	$\mathbf{v}^0$-$\mathbf{v}^8$-$\mathbf{v}^{10}$-$\mathbf{v}^{14}$-$\mathbf{v}^{15}$-$\mathbf{v}^{14}$-$\mathbf{v}^{10}$-$\mathbf{v}^8$-$\mathbf{v}^0$
S_{22}	-	$\mathbf{v}^0$-$\mathbf{v}^8$-$\mathbf{v}^{10}$-$\mathbf{v}^{11}$-$\mathbf{v}^{15}$-$\mathbf{v}^{11}$-$\mathbf{v}^{10}$-$\mathbf{v}^8$-$\mathbf{v}^0$
S_{23}	-	$\mathbf{v}^0$-$\mathbf{v}^8$-$\mathbf{v}^9$-$\mathbf{v}^{11}$-$\mathbf{v}^{15}$-$\mathbf{v}^{11}$-$\mathbf{v}^9$-$\mathbf{v}^8$-$\mathbf{v}^0$
S_{24}	-	$\mathbf{v}^0$-$\mathbf{v}^1$-$\mathbf{v}^9$-$\mathbf{v}^{11}$-$\mathbf{v}^{15}$-$\mathbf{v}^{11}$-$\mathbf{v}^9$-$\mathbf{v}^1$-$\mathbf{v}^0$

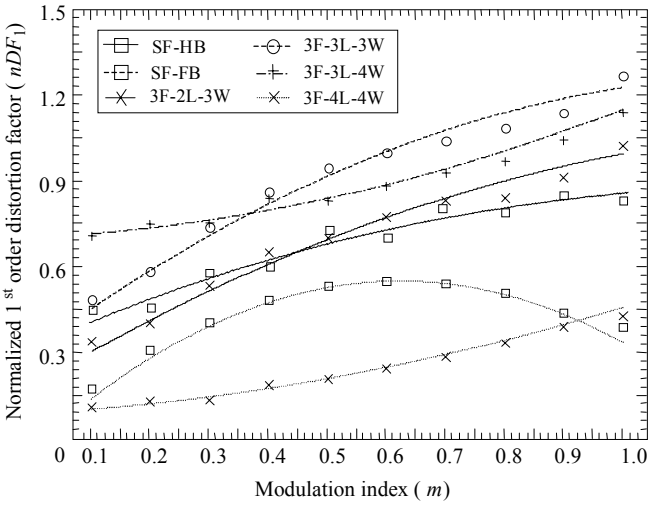

Fig.11. First-order normalized distortion curves (nDF_1)

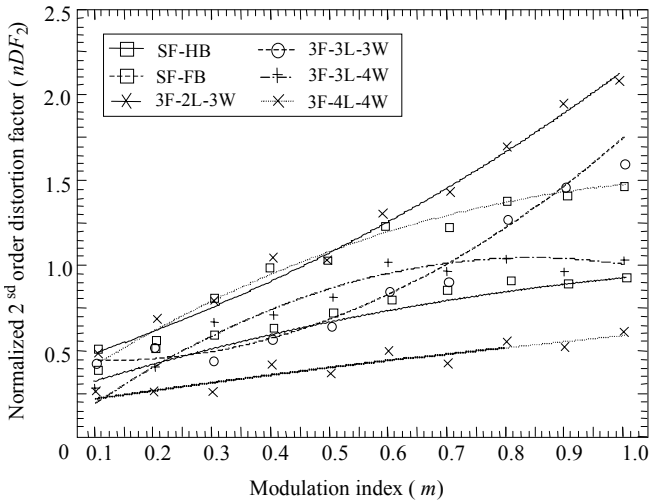

Fig.12. Second-order normalized distortion curves (nDF_2)

TABLE XI
Comparison between calculated and measured values of THD_v for a three-phase four-leg four-wire inverter

Test conditions	*m*	f_s (kHz)	L(μH)	C (μF)	THD_v (%) calculated	THD_v (%) measured
1	1	5	250	60	1.73	1.14
2	1	5	500	60	0.88	0.66
3	1	2.5	250	60	7.73	7.22
4	1	2.5	500	60	3.67	3.08
5	0.5	5	250	60	1.94	1.38
6	0.5	5	500	60	1.04	0.80
7	0.5	2.5	250	60	8.57	8.28
8	0.5	2.5	500	60	3.89	3.63

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APPENDIX
Boundary and separation "planes" of the three-phase two-leg three-wire converters

Sector	Boundary "Planes"	Separation "Planes"
S_1	$PL_1 \therefore u_\gamma + \sqrt{3}u_\delta - \sqrt{2}/2 = 0$	$u_\chi \geq 0$ and $u_\delta \geq 0$
S_2	$PL_1 \therefore u_\gamma - \sqrt{3}u_\delta - \sqrt{2}/2 = 0$	$u_\chi < 0$ and $u_\delta \geq 0$
S_3	$PL_1 \therefore u_\gamma + \sqrt{3}u_\delta + \sqrt{2}/2 = 0$	$u_\chi < 0$ and $u_\delta < 0$
S_4	$PL_1 \therefore u_\gamma - \sqrt{3}u_\delta + \sqrt{2}/2 = 0$	$u_\chi \geq 0$ and $u_\delta < 0$